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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,778	07/31/2003	Fong Shi	60000500.1012	7891

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EXAMINER	
CAO, PHAT X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 11/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/630,778	SHI, FONG	
	Examiner	Art Unit	
	Phat X. Cao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18 and 27-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-18,27-29,31,32 and 34* is/are rejected.

7)☒ Claim(s) *5,30 and 33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The cancellation of claims 19-26 in paper filed on 9/13/04 is acknowledged.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitation having a backside interconnect tied to "terminal pins" on the substrate recited in amended claim 1 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. Claim 18 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 18, a phrase "... a low dielectric having a dielectric constant of between about 2 GHZ and about 10 GHZ" is unclear. It is unclear because "GHZ" is not a unit for "a dielectric constant".

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-4, 7-12, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lai et al (US. 6,462,405) in view of Heckaman et al (US. 5,023,624).

Regarding claims 1-4, 12 and 14, Lai (Fig. 2) discloses a near-hermetic semiconductor device comprising: a substrate 40; an integrated circuit 41 disposed on the substrate 40; a lid or sealant 43 disposed on the integrated circuit 41; and a backside interconnect which includes plated-through vias formed in the substrate 40 (not shown, see column 4, lines 14-20), disposed on the integrated circuit 41, connecting the substrate 40 to the sealant-coated integrated circuit 41, and tied to terminal pins on the substrate (terminal pins corresponding to conductive traces formed

on the substrate (not shown), see column 4, lines 14-20); and a conformal coating 4 disposed on the sealant 43.

Lai does not disclose that the integrated circuit 41 is MMIC.

However, Heckaman (Fig. 1) teaches a hermetic device comprising an integrated circuit of MMIC or Phased Array Antenna (PAA) disposed on the substrate 20 (column 8, lines 40-50). Accordingly, it would have been obvious to form the integrated circuit of Lai as MMIC or PAA because it is an intended use depending upon the electronic application which is desired for the package device, as taught by Heckaman (column 8, lines 40-50).

Regarding claim 7, Heckaman further teaches the forming of a high performance support substrate (e.g., GaAs) for high frequency applications (column 1, lines 19-21).

Regarding claim 10, Lai's (Fig. 2) further discloses the solder attachment 42 formed along a periphery of the integrated circuit 41 to seal the integrated circuit 41 to the substrate 46.

Regarding claim 11, it would have been obvious to form the solder attachment 42 made of AuSn because AuSn is a well-known solder material which has a low melting point.

Regarding claim 8, Lai's (Fig. 2) further discloses that the device is substantially free of bond wires. It would have been obvious to substitute the solder balls 42 with the solder bumps because they are both well-known in the art for providing the electrical contacts between the chip and the substrate in the flip-chip technology.

Regarding claim 9, it would have been obvious to connect the plurality of rest vias of substrate 40 to the ground plane of the substrate in order to provide the external ground terminals for the device package.

6. Claims 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zuo et al (US. 6,525,420) in view of Chun et al (US. 6,710,542).

Zuo (Fig. 4) discloses a near-hermetic device comprising: a substrate 7; an electronic package 9 disposed on the substrate 7; a backside interconnect formed in the substrate 7, which connects the substrate 7 to the electronic package 9 (not shown, see column 4, lines 20-24); and an attached solder 13 to seal the electronic package 9 to the substrate 7.

Zuo does not disclose an interlayer dielectric disposed between a sealant and the electronic package.

However, Chun (Fig. 2) teaches a near-hermetic device comprising a sealant 22 disposed on the electronic package, and an interlayer dielectric 21 disposed between the sealant 22 and the electronic package. Accordingly, it would have been obvious to modify the semiconductor package of Zuo by forming the sealant and the interlayer dielectric with the structures as set forth above because as taught by Chun, such sealant and interlayer dielectric structures would provide a sealing layer which prevents the moisture and oxygen from reaching the electronic package (column 4, lines 11-17).

7. Claims 6, 27-29, 31-32 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zuo et al (US. 6,525,420) in view of Chun et al (US. 6,710,542) and Heckaman et al (US. 5,023,624).

Regarding claims 6 and 27-29, as discussed in details above, the combination of Zuo and Chun substantially reads on the invention as claimed, including the sealant 22 disposed over benzocyclobutene 21 (column 4, lines 9-21) for providing a sealing layer which prevents the moisture and oxygen from reaching the integrated circuit, as taught by Chun (see Fig. 2 and column 4, lines 11-17).

Neither Zuo nor Chun discloses that the integrated circuit is MMIC.

However, Heckaman (Fig. 1) teaches a hermetic device comprising an integrated circuit of MMIC or Phased Array Antenna (PAA) disposed on the substrate 20 (column 8, lines 40-50). Accordingly, it would have been obvious to form the integrated circuit of Zuo as MMIC or PAA because it is an intended use depending upon the electronic application which is desired for the package device, as taught by Heckaman (column 8, lines 40-50).

Regarding claim 31, Heckaman further teaches the forming of a high performance support substrate (e.g., GaAs) for high frequency applications (column 1, lines 19-21).

Regarding claim 32, Zuo (Fig. 4) further discloses the solder attachment 13 formed along a periphery of the integrated circuit 9 to seal the integrated circuit 9 to the substrate 7.

Regarding claim 34, Zuo (Fig. 4) also discloses a cover 20 disposed on the integrated circuit 9.

8. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lai et al (US. 6,462,405) in view of Okuaki (US: 4,814,943).

Lai (Fig. 2) discloses a hermetic semiconductor device, comprising: a substrate 40; an integrated circuit 41 disposed on the substrate 40; a sealant 43 disposed on the integrated circuit; a backside interconnect formed in the substrate 40 or 30 (not shown, see column 4, lines 14-20), which connects the substrate 40 to the sealant-coated integrated circuit; and a conformal coating 4 disposed on the sealant. It is noted that forming the integrated circuit 41 as a Monolithic Microwave Integrated Circuit (MMIC) would have been obvious because it is an intended use depending upon the electronic application which is desired for the package device.

Lai does not disclose a cover disposed on the package device without directly contacting the coating.

However, Okuaki (Fig. 8) teaches the forming of a cover 28 on the package device without directly contacting the coating 59. Accordingly, it would have been obvious to modify the package device of Lai by forming a cover with the structure as set forth above because as taught by Okuaki, such cover would provide a hermetically sealing for the package device (see abstract).

9. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lai et al and Heckaman et al as applied to claim 12 above, and further in view of Okuaki (US. 4,814,943).

Neither Lai nor Heckaman discloses a cover disposed over the conformal-coated integrated circuit in a con-contacting manner.

However, Okuaki (Fig. 8) teaches the forming of a cover 28 on the package device without directly contacting the coating 59. Accordingly, it would have been

obvious to modify the package device of Lai by forming a cover with the structure as set forth above because as taught by Okuaki, such cover would provide a hermetically sealing for the package device (see abstract).

Allowable Subject Matter

10. Claims 5, 30 and 33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

- in dependent claim 5, the prior art fails to disclose the combination of the semiconductor device structure as recited, including the sealant comprising a layer of silicon carbide having a thickness of about 4000 angstroms.
- in dependent claim 30, the prior art fails to disclose the combination of the semiconductor device structure as recited, including the sealant comprising a layer of silicon carbide.
- in dependent claim 33, the prior art fails to disclose the combination of the semiconductor device structure as recited, including a conformal coating disposed on the sealant.

Response to Arguments

11. Regarding claims 15-16, Applicant argues that the applied references fails to disclose an interlayer dielectric disposed between a sealant and an electronic package as amended.

Because this is a new issue, the new reference is applied in the new ground of

rejection to show the obviousness of forming an interlayer dielectric between a sealant and an electronic package.

Applicant further argues that the electronic package of Lai is not "a near-hermetic device".

This argument is not persuasive because the sealant 43 would function as a sealing layer because it completely covers the top surface of the chip 41. Furthermore, the encapsulant or the conformal coating 35 would result the hermetic sealing of the integrated circuit 41.

Regarding claims 1-4, 6-14, 17-18, 28-29, 31-32 and 34, because of the new issues, the new ground of rejection(s) is applied.

Conclusion

12. This action is made non-final.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is (571) 272-1703. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PC
November 29, 2004

PHAT X. CAO
PRIMARY EXAMINER